

## CLAIMS:

1. An arrangement for testing an integrated circuit comprising a combinational logic system (1), which arrangement performs a test of the behavior of the combinational logic system (1) in comparison with test software which emulates the nominal behavior of the integrated circuit, characterized in that the test software comprises two identical software models (11, 16) of the combinational logic system (1) to be tested, in which a test sample is applied for test purposes to a first (11) of these software models and whose output signals are coupled to a second (16) of these software models, in that the integrated circuit comprises a test circuit (2, 3, 4, 5) which, in a test mode, applies a test sample in a first test clock cycle to the input of the combinational logic system (1) of the integrated circuit and takes over the output signal in a buffer memory (2, 3, 4, 5), and which feeds back this test sample in a second test clock cycle to the input of the combinational logic system (1) and again takes over the output signal of the combinational logic system (1) in the buffer memory (2, 3, 4, 5), and in that, at the end of the second test clock cycle, the arrangement compares the results of the combinational logic system (1) of the integrated circuit in the buffer memory (2, 3, 4, 5) with the results of the second software model (16).

2. An arrangement as claimed in claim 1, characterized in that the buffer memory is constituted as a shift register (2, 3, 4, 5) by means of which the test samples are read and/or written.

3. A method of testing an integrated circuit comprising a combinational logic system (1), in which method the behavior of the combinational logic system (1) is compared with test software which emulates the nominal behavior of the integrated circuit, characterized in that the test software comprises two identical software models (11, 16) of the combinational logic system (1) to be tested, in which a test sample is applied for test purposes to a first (11) of these software models and whose output signals are coupled to a second (16) of these software models, in that the integrated circuit comprises a test circuit (2, 3, 4, 5) which, in a test mode, applies a test sample in a first test clock cycle to the input of the combinational logic system (1) of the integrated circuit and takes over the output signal in

- a buffer memory (2, 3, 4, 5), and which feeds back this test sample in a second test clock cycle to the input of the combinational logic system (1) and again takes over the output signal of the combinational logic system (1) in the buffer memory (2, 3, 4, 5), and in that at the end of the second test clock cycle, the results of the combinational logic system (1) of the
- 5 integrated circuit in the buffer memory (2, 3, 4, 5) are compared with the results of the second software model (16).

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